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I have completed on a project making physical logic gates and am now looking for a way to turn an arbitrary program into some series of logic gates so I can use them.
<http://stackoverflow.com/questions/30612124/logic-synthesis-from-an-arbitrary-piece-of-code>

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VHDL Tutorial: Learn by Example - University of -

VHDL Tutorial: Learn by Example (VHSIC Hardware Description Language) Logic synthesis offers an automated route from an RTL design to a Gate-Level design.

<http://esd.cs.ucr.edu/labs/tutorial/>

VHDL - Wikipedia, the free encyclopedia -

The next step was the development of logic synthesis tools that read the VHDL, of synthesizable VHDL code, the VHSIC Hardware Description Language or

<http://en.wikipedia.org/wiki/VHDL>

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