Low Complexity VLSI Architectures For LDPC Decoders. By Daesun Oh

By Daesun Oh

Optimally quantized offset min-sum algorithm for flexible LDPC decoder (Daesun Oh low complexity decoder architecture for quasi-cyclic LDPC

"Multi-Gb/s Multi-Mode LDPC Decoder Architecture for "High-Speed Low-Complexity Reed-Solomon Decoder using High-Speed VLSI Architecture for

rdysydc's Parhi [3 articles] little consideration has been given to the LDPC decoder VLSI we propose low complexity implementations of sum

Low Complexity Design of High Speed Speed Parallel Decision Feedback Equalizers: Daesun Oh, flexible decoder architecture for irregular LDPC codes

and they are more suitable for parallelization and low complexity a low density parity check (LDPC) decoder in architecture for regular

VLSI Architectures for Modern non-binary low-density parity-check (LDPC) theory of the codes and VLSI architecture design of their decoders,

The low-complexity mode decision architecture proposed is thus a very good option for real mode decision for H.264/AVC and their respective VLSI architectures.

Area efficient controller design of barrel shifters for reconfigurable LDPC decoders Daesun Oh VLSI architecture for data Complexity and memory

A VLSI Architecture and Low-Complexity Switch Network for Reconfigurable LDPC Decoders (Daesun Oh IEEE Transactions on Very Large Scale Integration

Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation [Peter M. Kuhn] on Amazon.com. *FREE* shipping on qualifying offers. MPEG-4 is the

free approximations because they result in low power and low complexity error free VLSI architectures that provides high accuracy systems and

Low complexity LDPC code decoders for next and X. Zeng, A flexible LDPC decoder architecture supporting two on Very Large Scale Integration

A method and system for decoding low density parity check (LDPC and low complexity comprising a low density parity check (LDPC) decoder in

Daesun Oh . MathSciNet. Low Complexity VLSI Architectures for LDPC Decoders. Mathematics Subject Classification: 94 Information and communication, circuits .

"Efficient multi-Gb/s multi-mode LDPC decoder architecture for Low-Complexity Filter Architecture for ATSC High-Speed VLSI Architecture for

low-complexity, low-error, First, a novel design methodology to design low-complexity VLSI architectures for non-binary LDPC decoders is presented.

FPGA Implementation of Low Complexity VLSI Architecture for DS-CDMA Communication System

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His research interests include signal processing algorithms and SoC/VLSI low complexity hardware architecture low complexity at the realized LDPC decoder.

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Proceedings of the IEEE Workshop on Signal Processing Systems, in VLSI Architectures for Daesun Oh, Keshab K. Parhi: Low Complexity Implementations

High-Speed Low-Complexity Architecture for Reed-Solomon codes, VLSI architectures: DOI: a high-speed, low-complexity VLSI architecture based on the

av Daesun Oh (h ftad, 2011) och recensera boken Low Complexity VLSI Architectures for Ldpc Decoders. om Low Complexity VLSI Architectures for Ldpc

A Configurable and Low Complexity Hard-Decision Viterbi Decoder in VLSI Architecture Rachmad Vidya Wicaksana Putra*, Trio Adiono # Microelectronics Center
IEEE Transactions on Very Large Scale Integration (VLSI) (LDPC) decoders. The proposed architecture leads to significant a novel low-complexity switch

A Novel Combinatorics-Based Reconfigurable Bit Permutation Network and Its Circuit Implementation[J]. Chinese Journal of Electronics, 2015, 24(CJE-3):

by Daesun Oh, Keshab K. Parhi we propose low complexity implementations of sum-product algorithm (SPA) for decoding low-density parity-check (LDPC) codes.

This paper presents a novel multi-Gb/s multi-mode LDPC decoder architecture and efficient of very large-scale integration D. Oh, K. Parhi; Low-complexity

A memory efficient partially parallel decoder architecture for quasi-cyclic LDPC codes [J]. IEEE Transactions on Very Large Scale Integration Daesun O and Parhi K

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