Low Complexity VLSI Architectures For LDPC Decoders. By Daesun Oh

By Daesun Oh

A method and system for decoding low density parity check (LDPC and low complexity comprising a low density parity check (LDPC) decoder in
http://www.google.nl/patents/US8418023

The subject of this dissertation is the design of VLSI architectures to Low Complexity, Low Power VLSI Architectures for complexity and power
http://citeseerx.ist.psu.edu/viewdoc/summary?doi=10.1.1.25.6606

A memory efficient partially parallel decoder architecture for quasi-cyclic LDPC codes [J]. IEEE Transactions on Very Large Scale Integration Daesun O and Parhi K
http://pub.chinasciencejournal.com/article/getArticleRedirect.action?doiCode=10.3724/SP.J.1146.2009.00388

This chapter provides first an overall survey of LDPC decoders, symbol-reliability-based message-passing decoding , low-complexity decoding for majority
http://www.sciencedirect.com/science/article/pii/B9780123964991000042

free approximations because they result in low power and low complexity error free VLSI architectures that provides high accuracy systems and
http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7042917

low-complexity, low-error, First, a novel design methodology to design low-complexity VLSI architectures for non-binary LDPC decoders is presented.
http://conservancy.umn.edu/handle/144408

"Efficient multi-Gb/s multi-mode LDPC decoder architecture for Low-Complexity Filter Architecture for ATSC High-Speed VLSI Architecture for
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Low Complexity Design of High Speed Speed Parallel Decision Feedback Equalizers: Daesun Oh, flexible decoder architecture for irregular LDPC codes
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codes have improved Very Large Scale Integration Fanucci, Low complexity LDPC code decoders for D Oh, K Parhi, Min-sum decoder architectures with
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A VLSI Architecture and Low-Complexity Switch Network for Reconfigurable LDPC Decoders (Daesun Oh IEEE Transactions on Very Large Scale Integration
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Low complexity LDPC code decoders for next and X. Zeng, A flexible LDPC decoder architecture supporting two on Very Large Scale Integration
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IEEE Transactions on Very Large Scale Integration (VLSI) (LDPC) decoders. The proposed architecture leads to significant a novel low-complexity switch
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High-Speed Low-Complexity Architecture for Reed-Solomon codes, VLSI architectures: DOI: a high-speed, low-complexity VLSI architecture based on the
http://adsabs.harvard.edu/abs/2010IEITI..93.1824L

A method and system for decoding low density parity check (LDPC and low complexity comprising a low density parity check (LDPC) decoder in
http://www.google.com/patents/US8656250

and they are more suitable for parallelization and low complexity a low density parity check (LDPC) decoder in architecture for regular
http://www.google.com/patents/US8359522

His research interests include signal processing algorithms and SoC/VLSI low complexity hardware architecture low complexity at the realized LDPC decoder.
http://etrij.etri.re.kr/etrij/journal/article/article.do?volume=36&issue=4+&page=591

IEEE Transactions on Very Large Scale Integration Low-complexity switch network for reconfigurable LDPC decoders: Daesun Oh,
http://dl.acm.org/citation.cfm?id=1825637.1825649&coll=DL&dl=GUIDE
A Configurable and Low Complexity Hard-Decision Viterbi Decoder in VLSI Architecture Rachmad Vidya Wicaksana Putra*, Trio Adiono # Microelectronics Center
http://www.academia.edu/9035499/A_Configurable_and_Low_Complexity_Hard-Decision_Viterbi_Decoder_in_VLSI_Architecture

Daesun Oh . MathSciNet. Low Complexity VLSI Architectures for LDPC Decoders. Mathematics Subject Classification: 94 Information and communication, circuits .
http://genealogy.math.ndsu.nodak.edu/id.php?id=157355
"Multi-Gb/s Multi-Mode LDPC Decoder Architecture for "High-Speed Low-Complexity Reed-Solomon Decoder using High-Speed VLSI Architecture for
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Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation [Peter M. Kuhn] on Amazon.com. *FREE* shipping on qualifying offers. MPEG-4 is the
http://www.amazon.com/Algorithms-Complexity-Analysis-Architectures-Estimation/dp/0792385160

Pris 1207 kr. K p Vlsi Architectures for Modern Error LDPC Decoder Architectures Scheduling Schemes VLSI Architectures for CNUs and VNUs Low
http://www.bokus.com/bok/9781482229646/vlsi-architectures-for-modern-error-correcting-codes/

The low-complexity mode decision architecture proposed is thus a very good option for real mode decision for H.264/AVC and their respective VLSI architectures.
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Efficient VLSI architectures for MIMO and cryptography It is of great interest to develop low-complexity and high-speed VLSI architectures for the MIMO
http://ir.library.oregonstate.edu/xmlui/handle/1957/7521

A Flexible LDPC/Turbo Decoder Architecture Yang Sun Low complexity LDPC code decoders for next IEEE Transactions on Very Large Scale Integration (VLSI
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