Low Complexity VLSI Architectures For LDPC Decoders. By Daesun Oh

By Daesun Oh

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Configurable M-factor VLSI DVB-S2 LDPC decoder -
codes have improved Very Large Scale Integration Fanucci, Low complexity LDPC code decoders for D Oh, K Parhi, Min-sum decoder architectures with

ETRI Journal -
His research interests include signal processing algorithms and SoC/VLSI low complexity hardware architecture low complexity at the realized LDPC decoder.

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"Multi-Gb/s Multi-Mode LDPC Decoder Architecture for "High-Speed Low-Complexity Reed-Solomon Decoder using High-Speed VLSI Architecture for

dblp: IEEE Workshop on Signal Processing Systems -
Proceedings of the IEEE Workshop on Signal Processing Systems, in VLSI Architectures for Daesun Oh, Keshab K. Parhi: Low Complexity Implementations

China Science Journal -
A memory efficient partially parallel decoder architecture for quasi-cyclic LDPC codes [J]. IEEE Transactions on Very Large Scale Integration Daesun O and Parhi K

Efficient VLSI architectures for MIMO and -
Efficient VLSI architectures for MIMO and cryptography It is of great interest to develop low-complexity and high-speed VLSI architectures for the MIMO

Algorithms, Complexity Analysis and VLSI -
Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation [Peter M. Kuhn] on Amazon.com. *FREE* shipping on qualifying offers. MPEG-4 is the

IEEE Xplore: Very Large Scale Integration (VLSI) -
IEEE Transactions on Very Large Scale Integration (VLSI) (LDPC) decoders. The proposed architecture leads to significant a novel low-complexity switch

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The subject of this dissertation is the design of VLSI architectures to Low Complexity, Low Power VLSI Architectures for complexity and power

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low-complexity, low-error, First, a novel design methodology to design low-complexity VLSI architectures for non-binary LDPC decoders is presented.

A Novel Combinatorics-Based Reconfigurable Bit -
A Novel Combinatorics-Based Reconfigurable Bit Permutation Network and Its Circuit Implementation[J]. Chinese Journal of Electronics, 2015, 24(CJE-3):

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CiteULike: rdysydc's Parhi [3 articles] -
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av Daesun Oh (h ftad, 2011) och recensera boken Low Complexity VLSI Architectures for Ldpc Decoders. om Low Complexity VLSI Architectures for Ldpc

IEEE Transactions on Very Large Scale Integration -
A VLSI Architecture and Low-Complexity Switch Network for Reconfigurable LDPC Decoders (Daesun Oh IEEE Transactions on Very Large Scale Integration

The Mathematics Genealogy Project - Daesun Oh -
Daesun Oh . MathSciNet. Low Complexity VLSI Architectures for LDPC Decoders. Mathematics Subject Classification: 94 Information and communication, circuits .

dblp: IEEE Transactions on Very Large Scale -
IEEE Transactions on Very Large Scale Integration (VLSI) Systems Daesun Oh, Keshab K. Parhi: Low-Complexity Switch Architecture for LDPC Decoder

VLSI Architectures for Modern Error-Correcting -
VLSI Architectures for Modern non-binary low-density parity-check (LDPC) theory of the codes and VLSI architecture design of their decoders,

Patent US8418023 - Low density parity check -
A method and system for decoding low density parity check (LDPC and low complexity comprising a low density parity check (LDPC) decoder in

A Configurable and Low Complexity Hard-Decision -
A Configurable and Low Complexity Hard-Decision Viterbi Decoder in VLSI Architecture Rachmad Vidya Wicaksana Putra*, Trio Adiono # Microelectronics Center

Efficient multi-Gb/s multi-mode LDPC decoder -
This paper presents a novel multi-Gb/s multi-mode LDPC decoder architecture and efficient of very large-scale integration D. Oh, K. Parhi; Low-complexity

2008 42nd Asilomar Conference on Signals, Systems -
Optimally quantized offset min-sum algorithm for flexible LDPC decoder (Daesun Oh low complexity decoder architecture for quasi-cyclic LDPC

CiteULike: rdysydc's Oh [2 articles] -
by Daesun Oh, Keshab K. Parhi we propose low complexity implementations of sum-product algorithm (SPA) for decoding low-density parity-check (LDPC) codes.

Low Complexity Design of High Speed Parallel -
Low Complexity Design of High Speed Speed Parallel Decision Feedback Equalizers: Daesun Oh, flexible decoder architecture for irregular LDPC codes

FPGA Implementation of Low Complexity VLSI -
FPGA Implementation of Low Complexity VLSI Architecture for DS-CDMA Communication System

Low- Complexity Hierarchical Mode Decision -

The low-complexity mode decision architecture proposed is thus a very good option for real mode decision for H.264/AVC and their respective VLSI architectures.